Amendments to the Drawings

Applicants respectfully present herewith replacement Figure 7A which includes the desired changes, without markings, and which comply with §1.84. The changes made to Figure 7A are explained in the accompanying remarks section below.

REMARKS

The Office Action dated December 29, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 17, 20, 22-24, 26, 30, 32, 36-41, 44-48, 50, 51, 53-63, 65, 66, 70-75, and 77-80 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 17-80 are pending in the present application and are respectfully submitted for consideration.

Drawings

Page 2 of the Office Action noted that, "Figures 6A-6B, 7A-7B, 8-12 and 15-17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated."

Replacement Figure 7A has been labeled --Prior Art--. As for the remaining figures noted above, Applicants respectfully traverse and submit that Figures 6A-6B, 7B, 8-12 and 15-17 are NOT old and do not warrant the label of --Prior Art--.

In particular, it is submitted that the specification describes Figs. 6A-6B, 7B, 8 to 12 and 15 to 17 as "Related Art" rather than "Prior Art." Specifically, Figs. 6A-6B, 7B, 8-12 are included in Japanese Unexamined Patent Publication (Kokai) No. 10-275038 (Japanese Patent Application No. 9-262507: JPA' 507) published on October 13, 1998, which corresponds to U.S. Patent Nos. 6,157,688 (USP '688), 6,377,638 and 6,493,394. Concretely, Figs. 6A-6B of this case substantially correspond to Figs. 125A-125B of USP' 688, Figs. 8-11 of this case substantially correspond to Figs. 140-143 of USP' 688, and Fig. 12 of this case substantially corresponds to Fig. 145 of USP' 688.

Please note that Figs. 15 to 17 (and 7A-7B) do not directly correspond to any drawings of USP'688, but they can be substantially read from USP' 688.

Furthermore, the application date of the basic application (Japanese Patent Application No. 9-318572: JPA'572) of this case is November 19, 1997, and the application date of the parent U.S. Application (Serial No. 09/062,586) of this case is April 20, 1998. On the other hand, the publication date of JPA'507 (JP-10-275038-A) is October 13, 1998, and the issue date of USP '688 (the earliest issued U.S. Patent) is December 5, 2000, and the publication date of corresponding DE application (DE-19744620-A1: DE'620) is May 20, 1998. Further, Japanese Patent Application Nos. 8-265844 (JPA'544) and 9-18907 (JPA'907), which are also basic applications of USP'688, are not published in Japan, since JPA'544 and JPA'907 are basic applications of a domestic priority application (JPA'507). Therefore, the application date (November 19, 1997) of JPA'572 and the application date (April 20, 1998) of the parent U.S. Application (Serial No. 09/062,586) of this case are both earlier than the publication date of DE'620 (the earliest publication date).

Consequently, Figs. 6A-6B, 7B, 8-12 and 15-17 of this case are not "Prior Art" nor admitted prior art, but is clearly disclosed as "Related Art." Thus, Applicants submit that Figures 6A-6B, 7B, 8-12 and 15-17 of the present application do not require the label of --Prior Art--.

Specification

The specification has been amended to include a cross-reference to the related application of U.S. application Serial No. 09/062,586, filed April 20, 1998, now U.S. Patent No. 6,185,256.

Formal Rejections to Claims

Claims 26, 32, 36, 44, 50, 57-63 and 77 were objected to as containing some minor informalities. Furthermore, claims 17-80 were rejected under 35 U.S.C. § 112, first paragraph and second paragraph.

Claims 17, 20, 22-24, 26, 30, 32, 36-41, 44-48, 50, 51, 53-63, 65, 66, 70-75, and 77-80 have been amended to correct the informalities noted in the Office Action, and have been amended to provide proper antecedent basis for the phrases recited in the claims, and to include the word "comprising" within the claims. Accordingly, Applicants submit that the claims are in compliance with US patent practice.

As for the rejection of claims 17-80 based on 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement, Applicants submit that each of the claims are fully supported the disclosure of the present application. For example, claims 17 and 65 correspond to Fig. 68 or the 12th embodiment of the disclosure, claim 20 relates to Figs. 13 to 20 or the first and second embodiments of the present disclosure, claim 40 relates to Fig. 21 or the third embodiment, claim 48 relates to Figs. 36-40 or the seventh and eighth embodiments, and claim 56 relates to Fig. 50 or the 10th embodiment of the present disclosure.

As such, Applicants respectfully request withdrawal of the objections and rejections.

Claims 17-19, 65 and 69 Rejected Under 35 U.S.C. § 102(e)

Claims 17-19, 65 and 69 were rejected under 35 U.S.C. § 102(e) as being anticipated by Akiyama et al. (U.S. Patent No. 5,638,335, hereinafter "Akiyama").

Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 17 recites a signal transmission system comprising, among other features, wherein, when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier.

Claim 65 recites a semiconductor memory device comprising, among other features, when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Akiyama as disclosing "a memory device in Figure 3 comprising a memory array having a plurality of bits and a plurality of memory blocks."

Applicants submit that Akiayama fails to disclose or suggest each and every element recited in claims 17 and 65 of the present application. In particular, it is submitted that the memory device of Akiyama is neither comparable nor analogous to

the semiconductor memory device and the signal transmission system of the present invention.

For instance, Akiyama merely relates to a semiconductor memory having a parity bit, wherein the number of memory blocks is determined to be an integral multiple of three [nx3] (generally the number of memory blocks is 2^n), and input/output bits of a memory array are changed while maintaining the bit structure of the memory blocks, with shortening the wiring length for the parity bit data, or without increase in propagation delay time. Specifically, a write operation to write data into a memory cell of Akiyama is merely performed in the conditions where the memory cell, bit lines, sense amplifier, and write amplifier are all electrically connected.

On the other hand, when performing the writing operation of the present invention, at least during portion of a period when a select signal for connecting a data bus to a sense amplifier is being supplied, a bit line connected to the sense amplifier is being supplied, a bit line connected as a load from the sense amplifier for amplification is disconnected as a load from the sense amplifier. For example, page 71, line 8 through page 73, line 4 of the present disclosure, data inversion in each sense amplifier can be performed at high speed since the sense amplifiers are not connected to respective bit line pairs. Thereafter, the sense amplifiers of the present invention are connected to corresponding memory cells via respective bit line pairs so as to write data into the corresponding memory cells. As such, it is submitted that Akiyama is different from the present invention and does not teach or suggest each and every feature recited in claims 17 and 65 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Akiyama fails to disclose or suggest each and every feature of claims 17 and 65. Accordingly, Applicants respectfully submit that claims 17 and 65 are not anticipated by nor rendered obvious by the cited prior art. Therefore, Applicants respectfully submit that claims 17 and 65 are allowable.

As claims 18-19 depend from claim 1, and claim 69 depends from claim 65, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claim 48 Rejected Under 35 U.S.C. § 102(e)

Claim 48 was rejected under 35 U.S.C. § 102(e) as being anticipated by Kurtze et al. (U.S. Patent No. 6,105,083, hereinafter "Kurtze"). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 48 recites a semiconductor memory device comprising, among other features, a state latch circuit for holding at least two states consisting of a CURRENT state indicating a bus currently in an active state and a NEXT state indicating a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating a bus in a standby state, and a PREVIOUS state indicating a bus just deactivated.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Kurtze merely discloses an interface enabling asynchronous data processing elements to be interconnected using an interconnection protocol, and wherein control information is double buffered and has two states, an "active" state and a "shadow" state. As clearly described on column 9, lines 56 through 59 of Kurtze, the active state contains the current state used in processing, while the shadow state is the control information for the next function to be performed. It is submitted that the "active" and "shadow" states of Kurtze constitute a queue of operations to be performed in the processing elements, and therefore, when the current "active" operation is completed, the queue proceeds one stage and the information stored in the "shadow" register becomes active. Therefore, the contents of the "active" and "shadow" registers of Kurtze may be consistent or different, and when the contents of the "active" and "shadow" registers are the same, the same operation is continuously performed in Kurtze.

In contrast, the present invention provides a semiconductor memory device with a state latch circuit for holding at least two states consisting of a CURRENT state indicating a bus currently in an active state and a NEXT state indicating a bus to be selected and activated next, or four states consisting of the CURRENT state, the NEXT state, or a STANDBY state indicating a bus in a standby state ready for selection after next, and a PREVIOUS state indicating a bus just deactivated. It is submitted that the state latch circuit of the present invention may hold two states, i.e., "CURRENT" and "NEXT." However, the CURRENT state of the present invention indicates a bus

currently in an active state and the NEXT state indicates a bus to be selected and activated next, and the operation of each state is previously determined.

Furthermore, the two states of present invention do not constitute a queue, as described in Kurtze. Rather, they correspond to states of a state machine where an operation to be performed in each state is previously determined. Thus, according to the present invention, each of the memory banks included in the memory array can be continuously operated like pipeline processing.

However, the states of Kurtze are only an instruction queue, and in the present invention, when starting an operation (burst read or write operation), the state can be automatically changed, like a state machine. Therefore, Applicants submit that Kurtze is different from the present invention, and further submit that the prior art fails to disclose or suggest each and every feature recited in claim 48 of the present application.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Conclusion

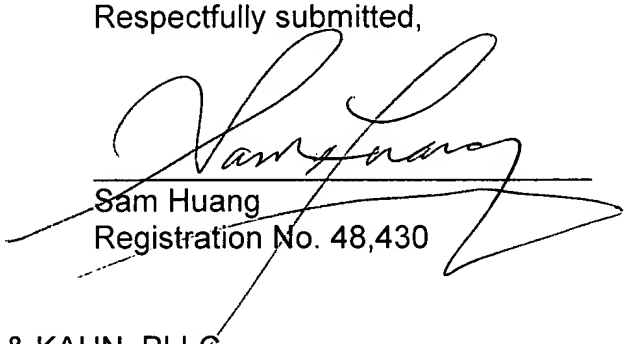
In view of the above, Applicants respectfully submit that each of claims 17-80 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 17-80 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the

Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Enclosure: Petition for Extension of Time (1 Month)